

**A METHOD FOR HIERARCHICAL SPECIFICATION  
OF SCHEDULING IN SYSTEM-LEVEL SIMULATIONS**

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**ABSTRACT OF THE DISCLOSURE**

A method for hierarchical specification and modeling of scheduling in system-level simulations. The invention addresses the specification aspect by introducing an explicit notion of a scheduler that must be designed as part of the system. A scheduler effectively represents a scheduling policy for an architectural resource. A scheduling policy governs how behaviors assigned to a resource, gain access and share the resource. The invention includes a general framework for modeling a scheduling policy, which includes a simple mechanism that covers many common cases. This framework is part of a Virtual Component Codesign (VCC) process, which is targeted at consumer embedded system design. Two orthogonal models, one of a scheduler and one of a schedulable, comprise the overall modeling of scheduling in the invention. The two models interact by sending messages to each other via a simple protocol. The protocol itself is implemented by a pair of abstract interfaces, which in turn are implemented in concrete schedulable and scheduler objects in the simulator.